METHOD OF FORMING GUARD RING PARAMETERIZED CELL STRUCTURE IN A HIERARCHICAL PARAMETERIZED CELL DESIGN, CHECKING AND VERIFICATION SYSTEM

Abstract

The invention displays a guard ring within an integrated circuit design by determining positions of the logic devices within the integrated circuit design, incorporating the guard ring into the integrated circuit design, and displaying the logic devices and the guard ring either graphically, semantically, or symbolically in a single display. The symbolic display comprises a parameterized symbol. The parameterized symbol displays parameters including the type of circuit, the type of guard ring and the efficiency of the guard ring. The invention displays the logic devices and the guard ring graphically by illustrating relative positions of the logic devices and the guard ring.